AMENDMENTS TO THE CLAIMS

1. (currently amended) A CMOS image sensor circuit, comprising:

a ~~first~~ CMOS image sensor chip comprising ~~including a chip substrate, said chip substrate having~~ an image sensor portion comprising ~~arranged in~~ an array of pixels ~~of~~ arranged in rows and columns, and a control portion comprising ~~with~~ image sensor logic ~~on said substrate~~, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first area and a second area;

said ~~substrate~~ chip being formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge;

said image sensor portion including imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said chip ~~substrate~~ and imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said chip ~~substrate~~;

said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion; and

a pixel interpolator and said chip driver circuitry located between said first area and said second area of said image sensor portion and said fourth edge of said chip ~~substrate; and~~

~~a second CMOS image sensor chip configured similarly to said first CMOS image sensor chip and abutted to one of said substrate edges of said first CMOS image sensor chip~~.

2. (previously presented) A circuit as in claim 1 wherein said row logic is formed in place of two columns of the array forming the image sensor portion.

3. (currently amended) A circuit as in claim 1 wherein said image sensor portion extends within two pixel pitches of said first, second, and third edges of the chip ~~substrate~~.

4. (original) A circuit as in claim 3 wherein said first and second edges are perpendicular to said third and fourth edges.

5. (previously presented) A circuit as in claim 1 wherein said pixel interpolater operates to interpolate pixels which would have been active in areas of said image sensor portions taken up by said row logic and by space between said CMOS image sensor portions.

6. (previously presented) A circuit as in claim 1 wherein said row logic is in the center of the plurality of pixels forming the image sensor portion.

7. (currently amended) A circuit as in claim 1, further comprising a guard ring formed around ~~wherein the ends of~~ the image sensor portion ~~include a guard ring~~.

8. (currently amended) A method of ~~operating a large format~~ capturing an image ~~sensor~~, comprising:

providing at least two ~~first obtaining an~~ image sensor ~~chip which has~~ chips, each chip having first and second edges and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array;

abutting said image sensor chips ~~chip against a similar image sensor chip of~~ along at least one of corresponding ~~construction~~ first and second edges; and

interpolating missing pixels on ~~chip~~ said chips, the missing pixels being caused by both said row select logic and by spaces between pixel pitches along abutted edges of said image sensor chips.

9. (currently amended) A CMOS imager, comprising:

a first CMOS image sensor chip having an image sensor portion arranged in an array of rows and columns, said first CMOS image sensor chip formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge; and

said first CMOS image sensor chip having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion and thereby forming at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor chip.

10. (currently amended) The CMOS imager according to claim 9, further comprising a second CMOS image sensor chip configured correspondingly ~~similarly~~ to said first CMOS image sensor chip and abutted to one of said edges of said first CMOS image sensor chip.

11. (currently amended) A method of fabricating a CMOS imager comprising:

fabricating at least two CMOS image ~~sensors~~ sensor chips having an image sensor portion arranged in an array of rows and columns, each of said at least two CMOS image ~~sensors~~ sensor chips formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge, said at least two image ~~sensors~~ sensor chips each having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array ~~forming~~ formed on said image sensor chip and thereby forming at least two image sensor areas for each of said at least two CMOS image

~~sensors~~ sensor chips, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said image sensor;

abutting said at least two CMOS image ~~sensors~~ sensor chips together; and

integrating said control portions of said at least two CMOS image ~~sensors~~ sensor chips such that said at least two CMOS image ~~sensors~~ chips function as a single CMOS imager.

12. (previously presented) The method of fabricating according to claim 11, further comprising interpolating, using said pixel interpolator of said control portion, missing pixels caused by said centralized row-local control portion and by spaces between said at least two image sensor areas.

13. (currently amended) A CMOS image sensor circuit, comprising:

a first CMOS image sensor chip ~~substrate, said substrate~~ having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said chip ~~substrate~~, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first area and a second area;

said first CMOS image sensor chip ~~substrate~~ formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel

edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge;

said first CMOS image sensor ~~substrate~~ portion extending between said first edge, said second edge, and said third edge, such that said first area of said image sensor portion is adjacent said first edge and said third edge of said image sensor chip ~~substrate~~ and said second area of said image sensor portion is adjacent said second edge and said third edge of said first CMOS image sensor chip ~~substrate~~;

said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion;

a pixel interpolator and said chip driver circuitry located between said first portion and said second portion of said image sensor portion and said fourth edge of said image sensor chip ~~substrate~~; and

a second CMOS image sensor chip ~~substrate~~ configured ~~similarly~~ correspondingly to said first CMOS image sensor chip ~~substrate~~ and abutted to one of said edges of said first CMOS image sensor chip ~~substrate~~.

Claims 14-16. (canceled)

17. (currently amended) A method of fabricating a CMOS imager comprising fabricating at least two CMOS image ~~sensors~~ sensor chips having an image sensor portion arranged in an array of rows and columns, each of said at least two CMOS image ~~sensors~~ sensor chips formed to have at least a first set of parallel edges including a first edge and a second edge, said a second set of parallel edges, different

than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge, each of said at least two image ~~sensors~~ sensor chips having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array ~~forming~~ formed on said image sensor chip and thereby forming at least two active image sensor areas in each of said at least two CMOS image ~~sensors~~ sensor chips, each said control portion respectively including a pixel interpolator located between said at least two image sensor areas and one of said edges of said image sensor chip.

18. (currently amended) The method according to claim 17, further comprising:

abutting said at least two CMOS image ~~sensors~~ sensor chips together; and

integrating said control portions of said at least two CMOS image ~~sensors~~ sensor chips such that said at least two CMOS image ~~sensors~~ sensor chips function as a single CMOS imager.

19. (previously presented) A circuit as in claim 1 wherein said row logic masks two columns of the array forming the image sensor portion.

20. (previously presented) A circuit as in claim 1 wherein said row logic is non-photosensitive.

21. (currently amended) A circuit as in claim 1 wherein ~~at least a portion of~~ said row logic ~~divides said image portion into said first and second areas~~ includes row drivers and row memory.

22. (previously presented) The CMOS imager according to claim 10, wherein the first and second CMOS image sensors are co-planar.